

Fig. 1 (Prior Art)

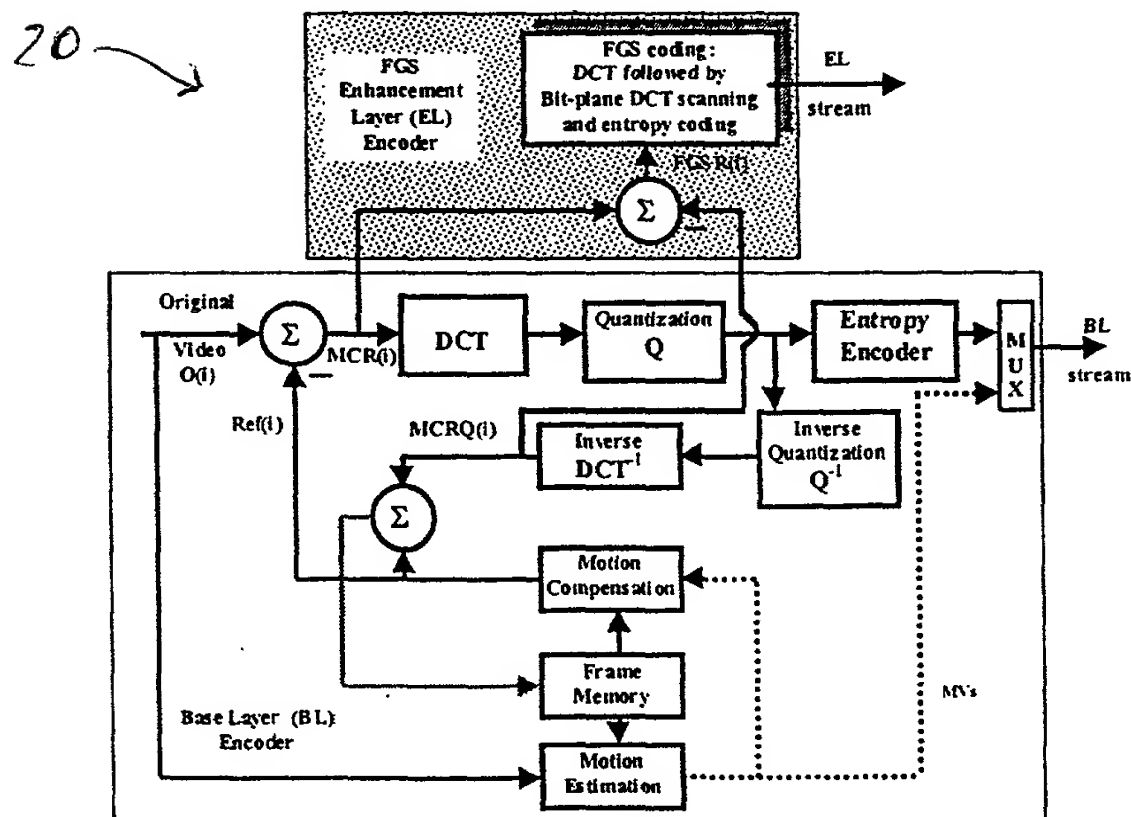


Fig. 2 (Prior Art)

30

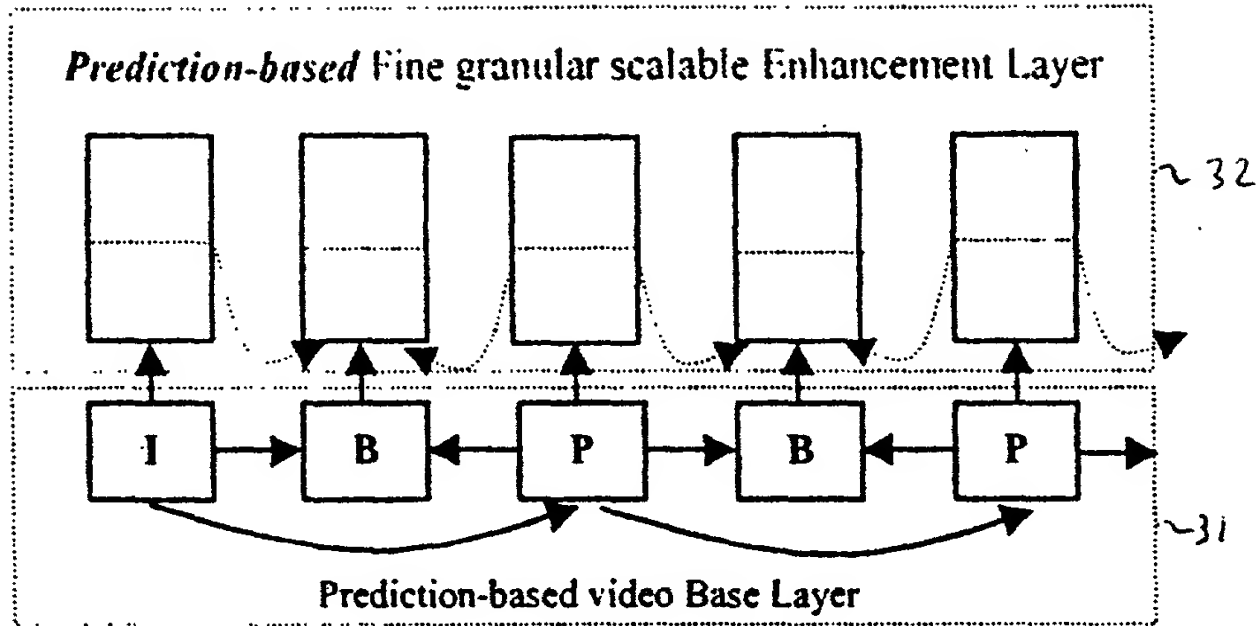


Fig. 3A

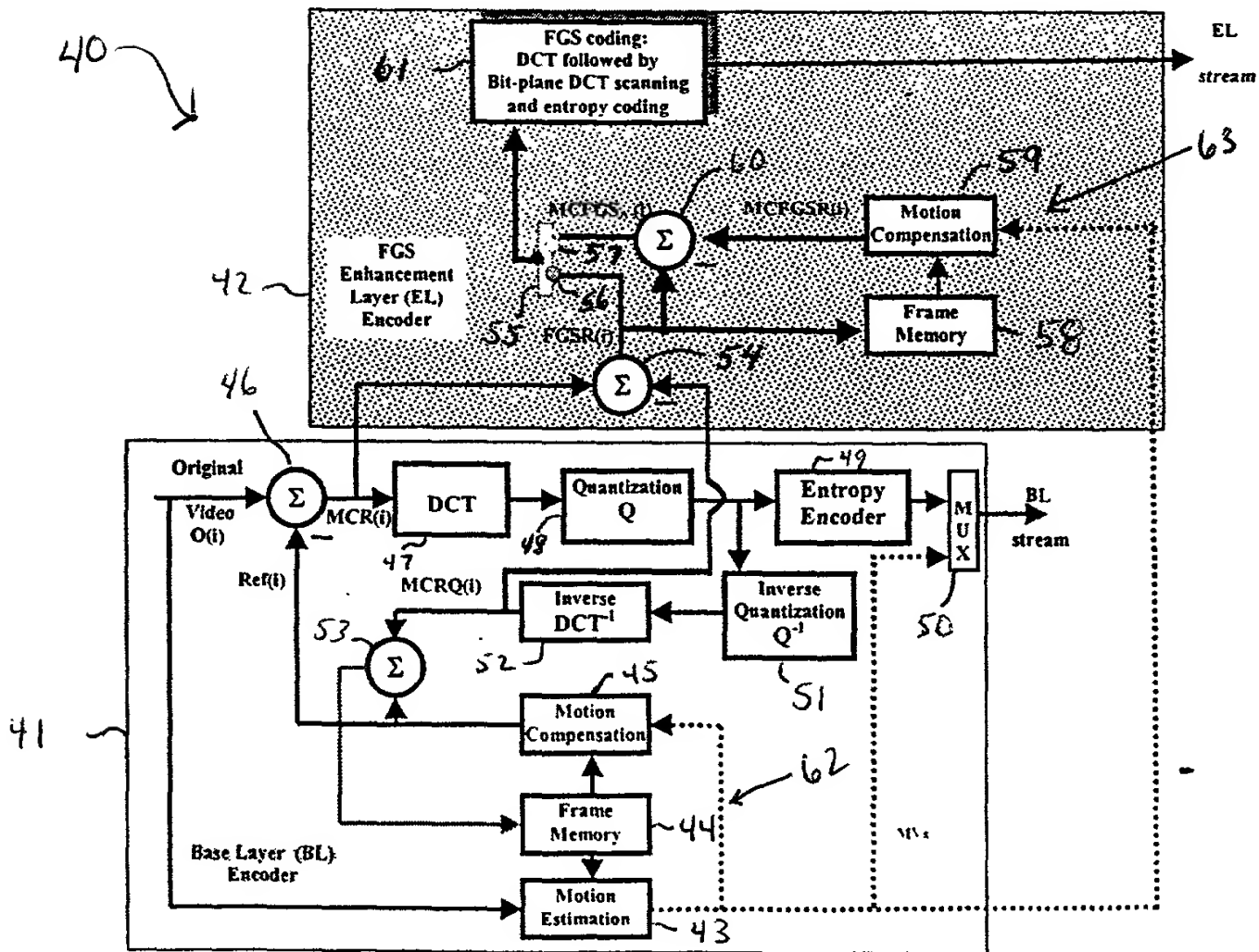
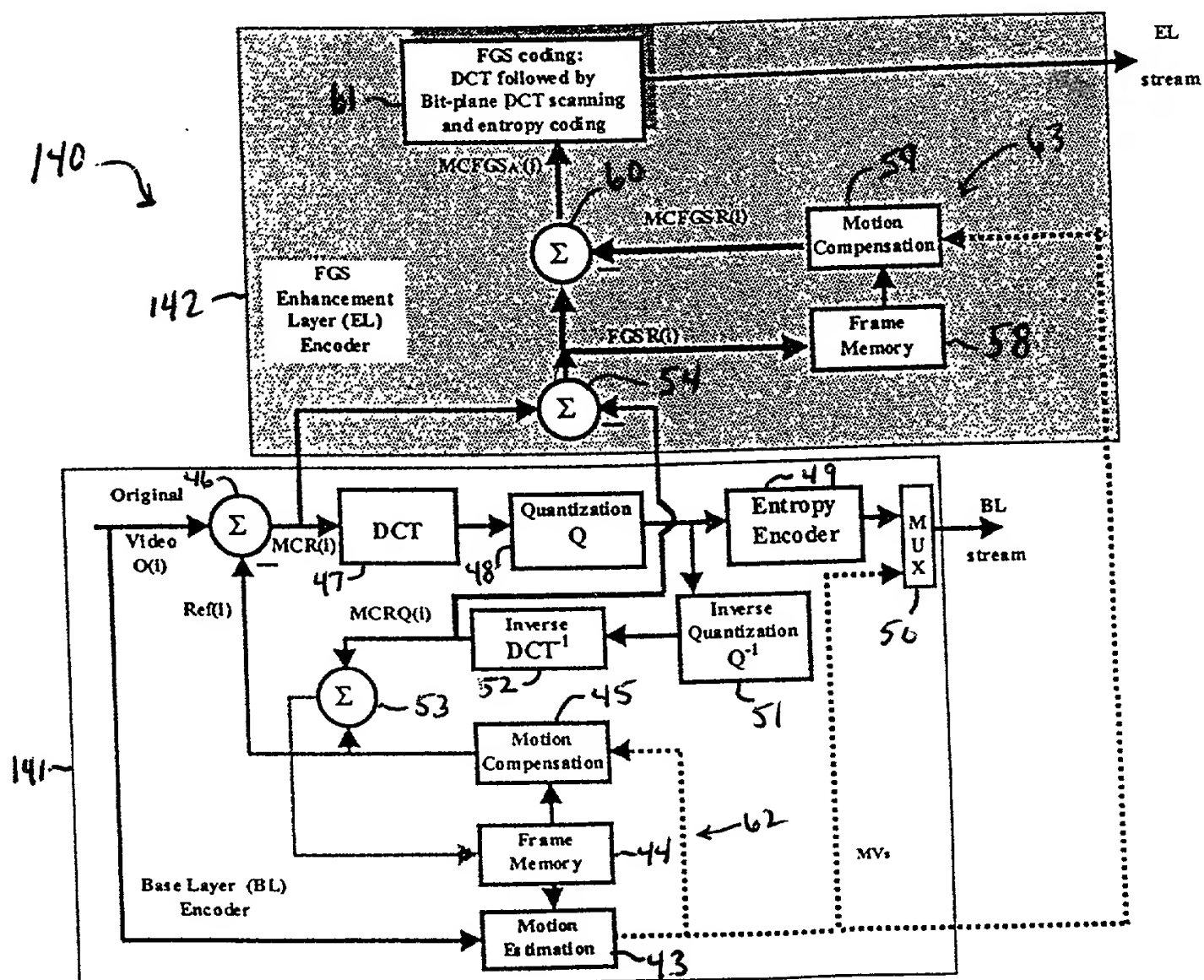
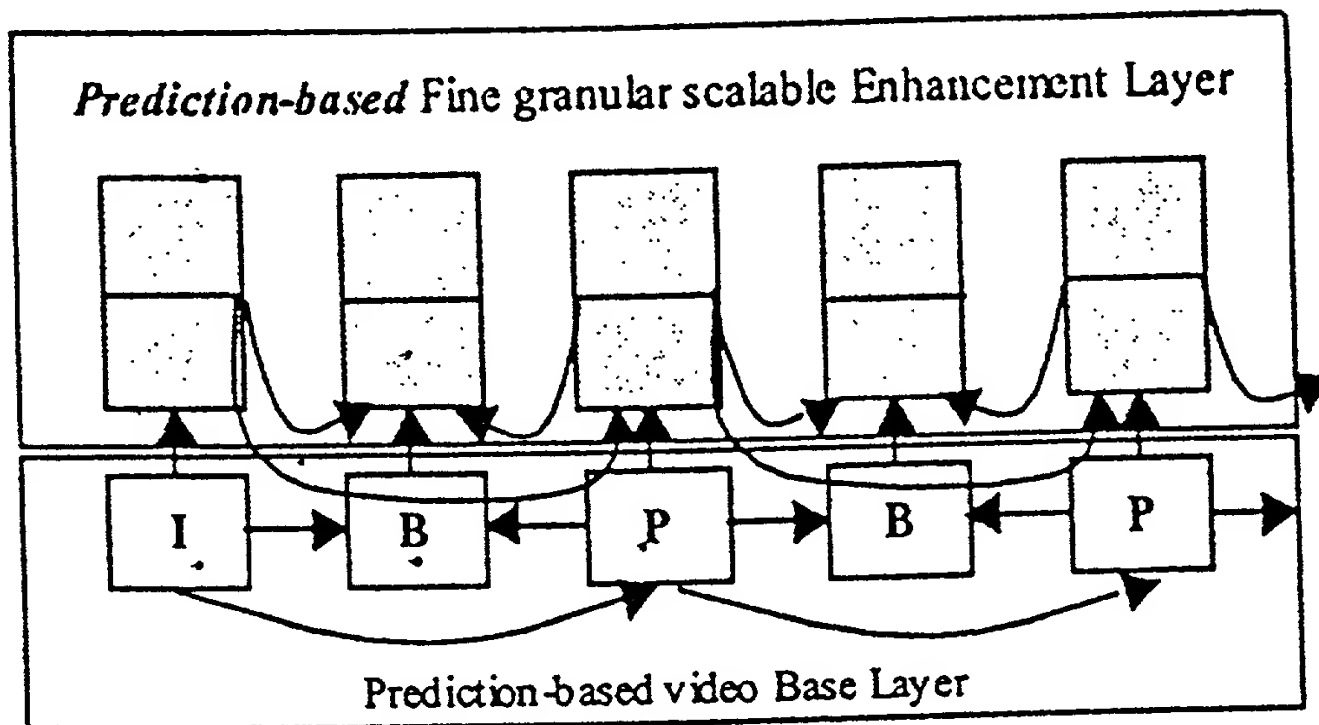


Fig 4



The diagram illustrates a video decoder architecture with two main processing paths: a Base Layer Decoder and an Enhancement Layer Decoder.

Base Layer Decoder (70):

- Input: **BL stream** (71).
- Processors: **De-MUX** (75), **Base Layer VLD** (83), **Inverse Quantization Q^{-1}** (84), and **Inverse DCT** (85).
- Memory: **Base Layer Frame Memory** (79).
- Output: **BL Video (optional)** (82).

Enhancement Layer Decoder (70):

- Input: **EL stream** (73).
- Processors: **FGS Bit-plane decoding** (86), **Motion Compensation** (88), and **Motion Compensation** (90).
- Memory: **Enh. layer Frame Memory** (87).
- Summing Junctions: Σ (92) and Σ (89).
- Output: **Enhanced Video** (89).

Inter-layer Interactions:

- Motion Vectors (MV's):** (76) are passed from the Base Layer Decoder to the Enhancement Layer Decoder.
- Motion Compensation:** The Base Layer Decoder's Motion Compensation (78) provides input to the Enhancement Layer Decoder's Motion Compensation (90).
- Summing:** The output of the Base Layer Decoder's Inverse DCT (85) is summed (81) with the output of the Enhancement Layer Decoder's Motion Compensation (90) at junction Σ (82). The result (80) is then summed (88) with the output of the FGS Bit-plane decoding (86) at junction Σ (89) to produce the final **Enhanced Video** (89).

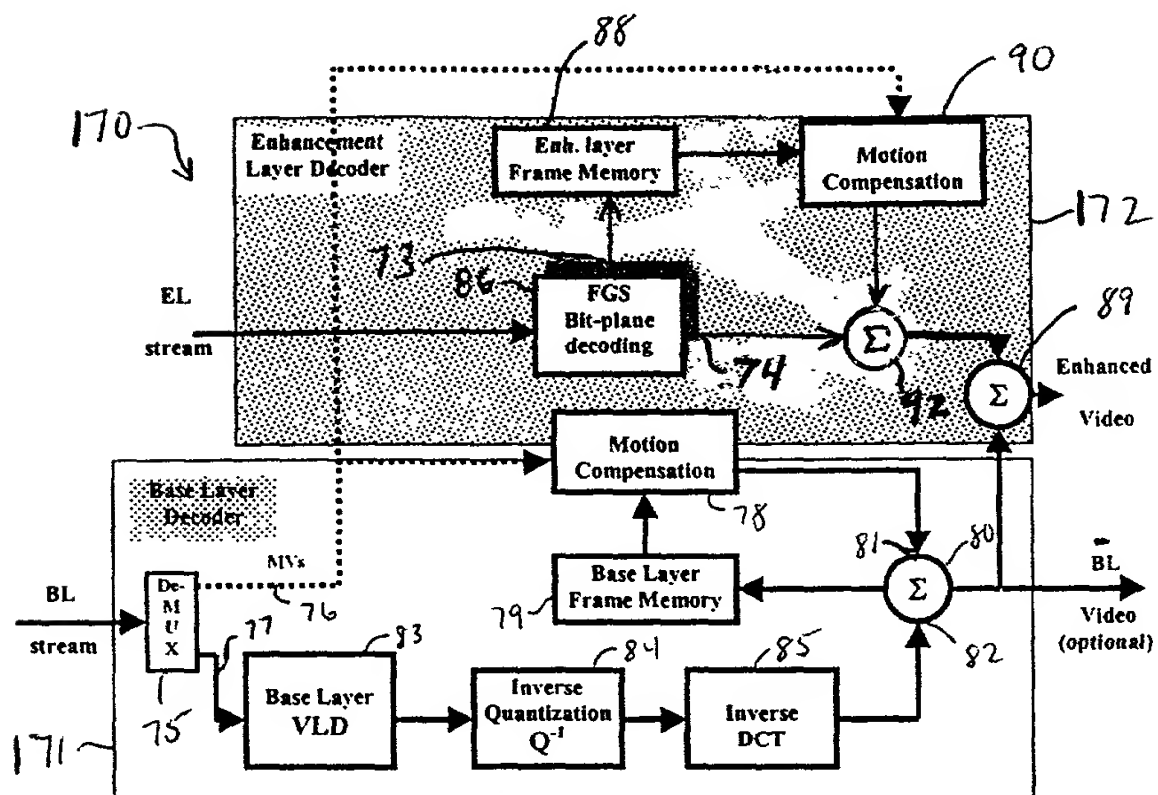


FIG. 8

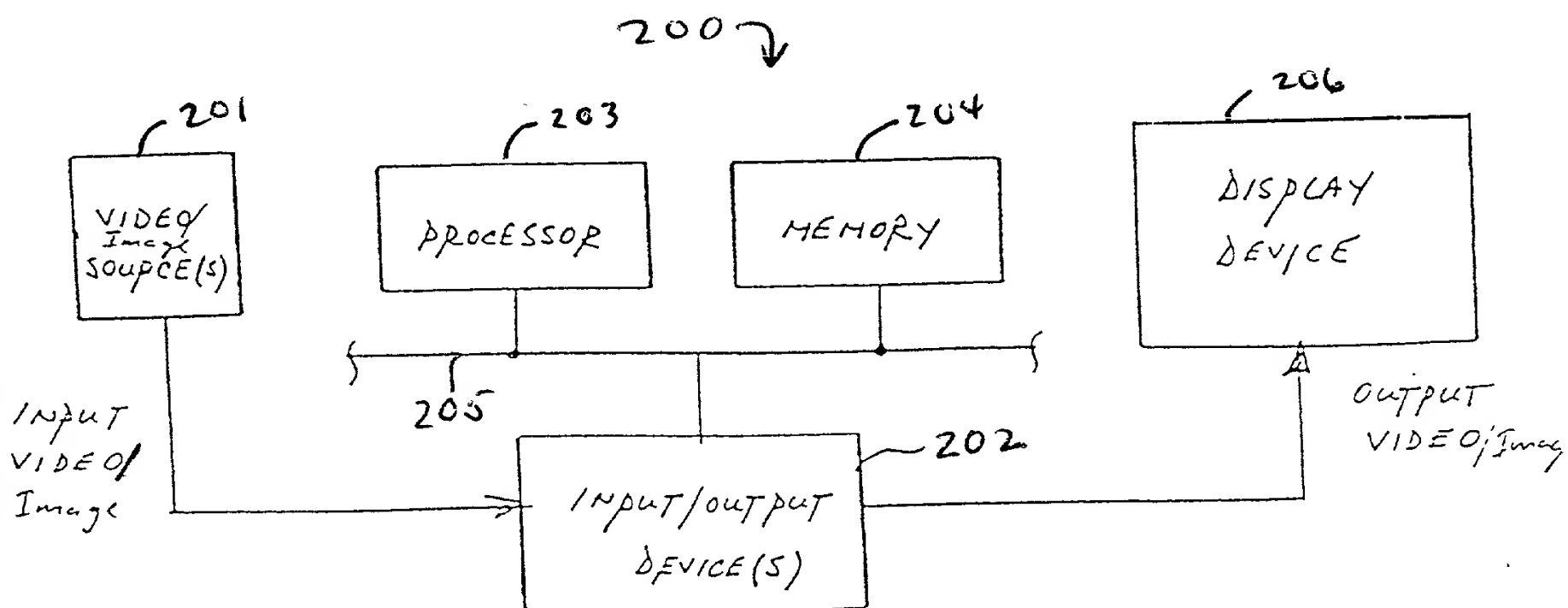


Fig. 8